AMENDMENTS

IN THE CLAIMS:

Please amend claims 1, 9, 16, 20 and 22 as follows:

1. (Twice Amended) A linear ramp generation circuit operating in a recovery mode, a ramp mode, or a hold mode, said circuit comprising:

an output node;

a first input node coupled to an externally provided first input signal;

a second input node coupled to an externally provided second input signal;

a constant current source network;

a capacitor having a first node and a second node, the first node being maintained at a circuit reference level, the second node being coupled to the output node at least during the hold mode of operation;

a return charge network for returning a voltage on the capacitor to a baseline level during the recovery mode, the return charge network including an active negative feedback circuit which exhibits analog behavior for regulating the voltage on the capacitor [analog active feedback circuit];

a first switch means responsive to the first input signal for connecting the second node of the capacitor to the constant current source network during the ramp mode of operation and changing the voltage on the capacitor away from the baseline level, and for uncoupling the second node of the capacitor from the constant current source network during the hold mode and recovery mode of operation; and

a second switch means responsive to the second input signal for connecting the second node of the capacitor to said return charge network during the recovery mode of operation to return the voltage on the capacitor to the baseline level, and for uncoupling the second node of the capacitor from the return charge network during the ramp mode and hold mode of operation.

9. (Twice Amended) A linear ramp generation circuit operating in a discharge mode, a hold mode, or a recovery mode, said circuit comprising:

a first input node and a second input node for receiving a first input signal and a second input signal, respectively;

an output node;

a constant current source network;

a recharge network including an [analog] active negative feedback circuit which exhibits analog behavior, the recharge network having a first recharge node and a second recharge node, the first recharge node connected to the output node;

a capacitor having a first capacitor node and a second capacitor node, the first capacitor node being maintained at a circuit reference level, and the second capacitor node being coupled to the output node at least during the hold mode of operation;

a first transistor switch responsive to the first input signal for connecting the second capacitor node to the constant current source network during the discharge mode of operation and for uncoupling the second capacitor node from the constant current source network during the hold mode and recovery mode of operation; and

a second transistor switch responsive to the second input signal for connecting the second capacitor node to the second recharge node during the recovery mode of operation and for uncoupling the second capacitor node from the second recharge node during the discharge mode and hold mode of operation.

16. (Twice Amended) A linear ramp generation circuit for operating in a ramp mode, a hold mode, or a recovery mode, said circuit comprising:

a first input node and a second input node for receiving a first input signal and a second input signal, respectively;

an output node;

a current network providing a constant current;

a return charge network including an [analog] active negative feedback circuit which exhibits analog behavior the recharge network having a first recharge node connected to the output node and a second recharge node connected to a control node;

a capacitor having a first capacitor node and a second capacitor node, the first capacitor node being maintained at a circuit reference level, and the second capacitor node being coupled to the output node at least during the hold mode of operation; and

a current steering element responsive to the first input signal for connecting the current network to the second capacitor node during the ramp mode of operation and for connecting the current network to a different node during the hold mode and recovery mode of operation.

20. (Amended) A method of sequentially operating a linear ramp generation circuit, said method comprising the steps of:

upon the occurrence of a first input signal, discharging a capacitor having a first node and a second node from an initial baseline voltage level by connecting a constant current source network to the second node of the capacitor, said first node being maintained at a circuit reference level;

upon the occurrence of a second input signal, disconnecting the second node of the capacitor from the constant current source network;

maintaining the second node of the capacitor at a high impedance during a hold period after the occurrence of the second input signal;

connecting the second node of the capacitor during the hold period to an output node;

upon the occurrence of a third input signal, connecting the second node of the capacitor to a recovery network including an active negative feedback circuit which exhibits analog behavior for recharging the capacitor back to the baseline voltage level; and

upon the occurrence of a fourth input signal, disconnecting the first node of the capacitor from the recovery network prior to a succeeding first input signal.

22. (Amended) A method of sequentially operating a linear ramp generation circuit, said method comprising the steps of:

upon the occurrence of a first input signal, discharging a capacitor having a first node and a second node from an initial baseline voltage level by connecting a constant current source network to the second node of the capacitor, said first node being maintained at a circuit reference level;

upon the occurrence of a second input signal, disconnecting the second node of capacitor from the constant current source network;

maintaining the second node of the capacitor at a high impedance during a hold period after the occurrence of the second input signal;

connecting the second node of the capacitor during the hold period to an output node;

upon the occurrence of a third input signal, connecting the second node of the capacitor to a recovery network including an [analog] active negative feedback circuit which exhibits analog behavior for recharging the capacitor back to the baseline voltage level; and

upon the occurrence of a fourth input signal, disconnecting the first node of the capacitor from the recovery network prior to a succeeding first input signal.

REMARKS

This Amendment and Response is in reply to the Final Office Action dated November 10, 1999. For the reasons more fully outlined below and in the original specification, Applicants respectfully submit that the claims now pending are in condition for allowance and respectfully request reconsideration and withdrawal of all rejections.

After the amendments and added claim, claims 1–16 and 18–22 are pending. Claims 1, 9, 16, 20, and 22 are independent.

At paragraph 3 of the Office Action, the Examiner objected to the claims for certain informalities. The amendments have amended claims 1 and 9 as suggested by the Examiner. Applicants respectfully request that the objections be withdrawn in view of the amendments.